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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,933	03/16/2004	Akiyoshi Aoyagi	9319S-000670	2339
27572	7590	10/10/2006	EXAMINER	
HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 828 BLOOMFIELD HILLS, MI 48303			SANDVIK, BENJAMIN P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/801,933

Applicant(s)

AOYAGI, AKIYOSHI

Examiner

Ben P. Sandvik

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,8 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-5, 8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al (U.S. Patent #6781241), in view of Asada (U.S. Patent #6239496).

With respect to **claim 1**, Nishimura teaches a first carrier substrate (Fig. 6, 1b); a first semiconductor chip mounted face down on the first carrier substrate (Fig. 6, 3b); a second semiconductor chip mounted face down on a reverse face of the first carrier substrate (Fig. 6, 3f); a second carrier substrate (Fig. 6, 1a); a third semiconductor chip mounted on the second carrier substrate (Fig. 6, 3c); and protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip (Fig. 6, 7), such that a gap is created between the second carrier substrate and the first semiconductor chip (Fig. 6,

gap between second carrier substrate and first semiconductor chip is occupied by another chip); wherein the third semiconductor chip comprises a structure in which a plurality of chips are stacked (Fig. 6, 3c and 3d).

Nishimura does not teach a first anisotropic conductive sheet disposed between the first semiconductor chip and the first carrier substrate and having a first side and a second side, the first side of the first anisotropic conductive sheet being in contact with the first carrier substrate and a pair of lands and the second side of the first anisotropic conductive sheet having a first portion in contact with the first semiconductor chip and a second portion extending past the first semiconductor chip; or a second anisotropic conductive sheet disposed between the second semiconductor chip and the first carrier substrate and having a first side and a second side, the first side of the second anisotropic conductive sheet being in contact with the first carrier substrate and a pair of lands and the second side of the second anisotropic conductive sheet having a first portion in contact with the second semiconductor chip and a second portion extending past the second semiconductor chip.

Asada teaches a stacked package of carrier substrates (Fig. 8A/8B), each carrier substrate comprising an anisotropic conductive sheet provided between the substrate and a chip (Fig. 8A, 621), the first side of the sheet in contact with the substrate and a pair of lands (Fig. 8A, 611), the second side of the sheet having a first portion in contact with the chip (Fig. 8A, 131) and a second portion extending past the chip (Fig. 8A, sloped portion of anisotropic sheet 621); and a

gap between the second portion and subsequent carrier substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an anisotropic conductive sheet between the chips and carrier substrates of Nishimura as taught by Asada in order to only allow conduction in a direction perpendicular to the substrate.

With respect to **claim 3**, Nishimura teaches a sealant for sealing the third semiconductor chip (Fig. 6, 2).

With respect to **claim 4**, Nishimura teaches a sealant comprising molded resin (Col 7 Ln 29).

With respect to **claim 5**, Nishimura teaches that a position of a sidewall of the sealant coincides with a sidewall of the second carrier substrate (Fig. 6, 1a and 2).

With respect to **claim 8**, Nishimura teaches that the first carrier substrate comprises a flip-chip mounted ball grid array (Fig. 6, 8), and that the second carrier substrate comprises a mold-sealed ball grid array (Fig. 6, 9).

With respect to **claim 10**, Nishimura teaches that the third semiconductor chip comprises a structure in which a plurality of chips is arranged in parallel on the second carrier substrate (Fig. 6, 3c and 3d).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps


EVAN PERT
PRIMARY EXAMINER